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10/596,868	06/28/2006	Mark J. Childs	GB040006	1718

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EXAMINER	
ZHOU, HONG	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/596,868	CHILDS, MARK J.	
	Examiner	Art Unit	
	HONG ZHOU	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on January 17, 2009 has been entered. Claims 1 and 10 have been amended. Claims 1-13 are pending in this application, with claims 1 and 10 being independent claims.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 4-6, and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al (US 2005/0156829, hereinafter Choi) in view of Kane et al (US 6, 618,030, hereinafter Kane).

Regarding claim 1, Choi discloses an active matrix electroluminescent display device (Figs. 1 and 2) comprising an array of display pixels (140), each pixel comprising: an electroluminescent display element (OELD, Fig. 2); a drive transistor (M3, Fig. 2) for driving a current through the display element (OELD); an address transistor (M1, Fig. 2) for providing a pixel drive signal from a data line (110, Fig. 2) to the gate of the drive transistor (M3); and a shorting transistor (transistor M2, compensating the characteristic of the transistor M3 in response to a compensation signal SEL2, also see [0042-0046] at page 3) connected between the gate and drain of the drive transistor (M3) and storage capacitors (C1 and C2) are directly connected between a power supply line (VDD) and the gate of the drive transistor (M3).

In Fig. 2, Choi does not disclose using a single storage to maintain the data voltage supplied to the gate of the drive transistor and that wherein the display device further comprises means for measuring a voltage on the data line.

Choi in Fig. 11, however, discloses a single storage capacitor (C) directly connected between a power supply line (VDD) and the gate of a drive transistor (Mb). Choi teaches that the storage capacitor C is used for storing supplied data voltage for a predetermined time (see [0006]).

At the time of the invention it would have been obvious to one of ordinary skill in the art to modify the pixel circuit of Fig. 2 with the single storage capacitor C of Fig. 11 for keeping the data voltage applied to the gate of the drive transistor Mb for a predetermined time, because using a single storage capacitor instead of two storage capacitor would allow the costs associated with a display device to be reduced.

It is noted that Choi fails to disclose wherein the display device further comprises means for measuring a voltage on the data line.

However, Kane discloses an organic LED display device wherein the display device comprises a measuring module (1330, Fig. 13) for measuring the drive transistor's threshold voltage on a data line (data line 1210, Fig. 13; col. 4, lines 66-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the electroluminescent display device of Choi with the feature of a measurement module for measuring the voltage of a data line and adjusting the input pixel data as taught by Kane so as to improve brightness uniformity (col. 2, lines 14-17).

Regarding claim 2, Choi as modified by Kane further discloses a device as claimed in claim 1, wherein the EL display element (OELD) and the drive transistor (M3) are connected in series between first (Power line VDD) and second power lines (ground line, Fig. 2).

Regarding claim 4, Choi as modified by Kane discloses a device as claimed in claim 1, wherein the data input line (110) is switchable between a voltage driving mode in which it provides voltages to the pixels connected to the line (see [0043], page 3) and a floating mode in which it can float to the voltage of the gate of the drive transistor of an addressed pixel (see [0049], page 3).

Regarding claim 5, Choi as modified by Kane discloses a device as claimed in claim 1, wherein each pixel is operable in two modes: a first, threshold voltage measuring mode, in which the display element is disabled (e.g. during the auto-zero phase, the LED's turn-on voltage is measured, see col. 4, lines 66-67 of Kane), the address transistor (M1 of Choi) is turned on and the shorting transistor (M2 of Choi) is turned on; and a second, pixel drive mode (M3 is turned on in Choi), in which the display element is enabled, the address transistor (M1 of Choi) is turned on and the shorting transistor (M2 of Choi) is turned off (see [0043] and [0049] at page 3).

Regarding claim 6, Choi as modified by Kane discloses a device as claimed in claim 5, wherein during the first, threshold voltage measuring mode, during a first period a predetermined voltage is applied to the data line so that a current is driven through the drive transistor (see col. 4, line 64 to col. 5, line 12 of Kane) and during a second period the data line is allowed to float

so that the voltage on the data line (6) substantially follows the gate voltage of the drive transistor (see [0049], page 3 of Choi).

Regarding claim 9, Choi as modified by Kane discloses a device as claimed in claim 1, further comprising a storage capacitor (C2) between the gate and source of the drive transistor (M3) (Fig. 2).

Regarding claim 10, Choi discloses a method of addressing the pixels of an active matrix electroluminescent display device (Fig. 1 and Fig. 2), comprising an electroluminescent (EL) display element (OELD) and a drive transistor (M3, Fig. 2) for driving a current through the display element (OELD), the method comprising: disabling the display element (2); applying a first voltage to a data line (110); coupling a power supply line (VDD) directly to the gate of the drive transistor (M3) by storage capacitors (C1 and C2); driving a current through the drive transistor (M3, Fig. 2), through a shorting transistor (M2, Fig. 2) connected between the gate and drain of the drive transistor (M3, Fig. 3) and through an address transistor (M1) connected between the gate of the drive transistor (M3) and the data line (110, Fig. 2), allowing the data line (110) electrically float (see [0045] at page 3).

In Fig. 2, Choi does not disclose coupling the power supply line directly to the gate of the drive transistor by a single storage capacitor and the method further comprising measuring a voltage on the data line and modifying a data voltage to be applied to the drive transistor using the voltage measured on the data line.

Choi in Fig. 11, however, discloses a single storage capacitor (C) directly connected between a power supply line (VDD) and the gate of a drive transistor (Mb). Choi teaches that the storage capacitor C is used for storing supplied data voltage for a predetermined time (see [0006]).

At the time of the invention it would have been obvious to one of ordinary skill in the art to modify the pixel circuit of Fig. 2 with the single storage capacitor C of Fig. 11 for keeping the data voltage applied to the gate of the drive transistor Mb for a predetermined time, because using a single storage capacitor instead of two storage capacitor would allow the costs associated with a display device to be reduced.

It is noted that Choi fails to disclose the method further comprising measuring a voltage on the data line and modifying a data voltage to be applied to the drive transistor using the voltage measured on the data line.

However, Kane discloses an organic LED display device wherein the display device comprises a measuring module (1330, Fig. 13) for measuring the drive transistor's threshold voltage on a data line (data line 1210, Fig. 13; col. 4, lines 66-67) and modifying a data voltage to be applied to the drive transistor using the voltage measured on the data line (see Figs. 17 and 18).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the electroluminescent display device of Choi with the feature of a measurement module for measuring the voltage of a data line and adjusting the input pixel data as taught by Kane so as to improve brightness uniformity (col. 2, lines 14-17).

Regarding claim 11, Choi as modified by Kane discloses a method as claimed in claim 10, wherein disabling the display element comprising applying a disable voltage to a terminal of the display element (e.g. the OELD is connected to ground when the display element is disabling).

Regarding claim 12, Choi as modified by Kane discloses a method as claimed in claim 11, wherein disabling the display element comprising applying a disable voltage to terminal (34) of the display element (2) which is common to all display elements.

Regarding claim 13, Choi as modified by Kane discloses a method as claimed in claim 10, further comprising enabling the display element (e.g. when the drive M3 is turned "on"), and addressing the pixel with the modified data voltage on the data line (e.g. when the address transistor M1 is turned "on"), with the shorting transistor (e.g. transistor M2) turned off (see [0049] at page 3, the transistor M2 is cut off).

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al (US2005/0156829, hereinafter Choi) in view of Kane et al (US 6, 618,030, hereinafter Kane), and further in view of Libsch et al (US 7,167,169, hereinafter Libsch).

Regarding claim 3, Choi as modified by Kane discloses a device as claimed in claim 2. However, both Choi and Kane fail to wherein the voltage on the second power line is switchable between two values, one of which causes the EL display element (2) to be turned off. However, Libsch discloses an active matrix oled voltage drive pixel circuit including an organic light

emitting diode (550) and a drive transistor (Q2) connected in series between first (V1) and second power lines (V4). Libsch further discloses whererin the voltage (V4) on the second power line is switchable between twp values (e.g., 0V and 15V), and when the voltage is set to 15V the OLED is turned off.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the electroluminescent display device of Choi as modified by Kane with the features of different voltage levels in one terminal of the OLED as taught by Libsch so as to provide an AC driving for the OLED which would prolong the life of the OLED.

6. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi et al (US 2005/0156829, hereinafter Choi) in view of Kane et al (US 6, 618,030, hereinafter Kane), and further in view of Tokioka et al (US 7,079,094, hereinafter Tokioka).

Regarding claim 7, Choi as modified by Kane discloses a device as claimed in claim 1. Both Choi and Kane Choi fail to disclose wherein the drive transistor (22) is a polysilicon TFT.

However, Tokioka discloses an electroluminescence display (Fig. 7) using a low-polysilicon TFT as a drive transistor of an organic light emitting device (col. 1, lines 21-31).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the electroluminescent display device of Choi as modified by Kane with the feature of a low temperature polysilicon TFT as taught by Tokioka for driving the OLED because a driving transistor using low temperature polysilicon TFT provides higher definition of an image and lower power consumption (col. 1, lines 21-31).

Regarding claim 8, Tokioka further discloses a device as claimed in claim 7, wherein the drive transistor (22) is a low temperature polysilicon TFT (col. 1, lines 21-31).

Response to Arguments

7. Applicant's arguments filed January 27, 2009, with respect to the amendments to claim 1 and claim 11 have been fully considered but are moot in view of the new ground(s) of rejection.

On pages 7 and 8 of the Applicant's Remarks, the Applicant argues that the pixel circuit of Choi as shown in Fig. 2 does not teach coupling a power supply line directly to the gate of the drive transistor by a single storage capacitor as recited in the amended independent claim 1 and claim 10, but requires two storage capacitors C2 and C2. However, Fig. 11 and paragraph [0006] of Choi clearly discloses a single storage capacitor C directly connecting a power source line VDD to the gate of a drive transistor Mb for storing the data voltage supplied to the drive transistor Mb. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the single storage transistor instead of the two storage capacitor in the pixel circuit of Choi as shown in Fig. 2 in order to reduce the manufacturing costs of the display device.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HONG ZHOU whose telephone number is (571)270-5372. The examiner can normally be reached on Monday through Friday 8:30 A.M. - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571)272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/H. Z. /
Examiner, Art Unit 2629

/Amare Mengistu/

Supervisory Patent Examiner, Art Unit 2629